PSG5220/5210 Layout Guidlines

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Illustration Index

1 Current Sense connections:

1.1 Kelvin Connections:

If a 4 terminal Rsense is not used it is important to use Kelvin connections for the CS#+/- connections. These connections will ensure that as little current as possible flows down the return path to CS#+/-. Current on these traces will cause voltage error at the PSG5220 current sense inputs and may reduce the effectiveness of the part. Please see Illustration 1: Kelvin Connections for an example of how to make Kelvin connections. The separation of the smaller pad from the larger ones prevents current flow from interfering with the measurements.

1.2 Filter location:

The differential voltage from Rsense should be filtered with a differential RC filter. The capacitor for this filter should be located as close to CS#+/- as possible. This close proximity will reduce noise that could be coupled in after the filtering takes place, and allow the sensor to get a more accurate reading. Please see Illustration 2: Filter Placement for an example.

1.3 CS#+/- traces:

CS#+/- traces should be kept as short as possible and must be routed as a differential pair with an impedance matching that of the RC filter.

2 Ripple Injection Connections:

2.1 FB#:

The ripple injection signal is high frequency but low current. Since the FB# pins are located next to the sensitive current sense inputs, take care routing this signal to avoid coupling the ripple voltage and switching noise into them.

3 Gate signals:

The top gate signals have fast rise and fall times with associated high current pulses while turning on and off the external MOSFETs. The return path for TG is SW, so minimize area of the TG->MOSFET gate, MOSFET source->SW path. Subsequently, the return path for BG is the adjacent PGND pin, so minimize the area of the BG->MOSFET gate, MOSFET source->PGND path. It would be ideal to have equal length traces for TG and BG. You will want to keep the MOSFETs close to the gate drivers as well to reduce parasitics.

4 Power Path

The loop area for this high current path should be kept to a minimum. This high current path includes: Vin capacitors, top and bottom FETs, inductor, Rsense, and the Vout capacitors. The high current ground path should be connected to an internal ground plane at one point. This should be done in a typical star ground configuration. A star ground configuration will reduce ground bounce and reduce reference errors. Please see Illustration 6: Power Path for an example.

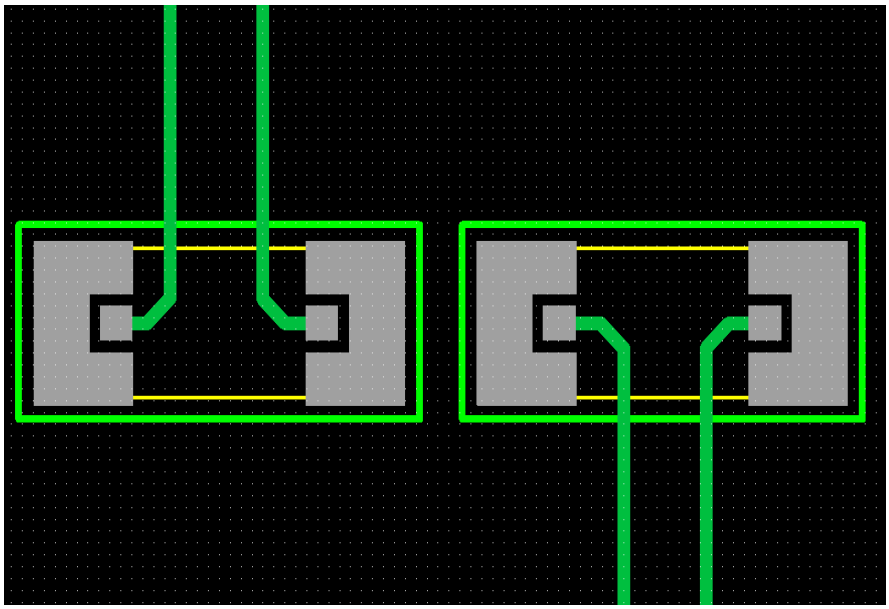

Illustration 1: Kelvin Connections

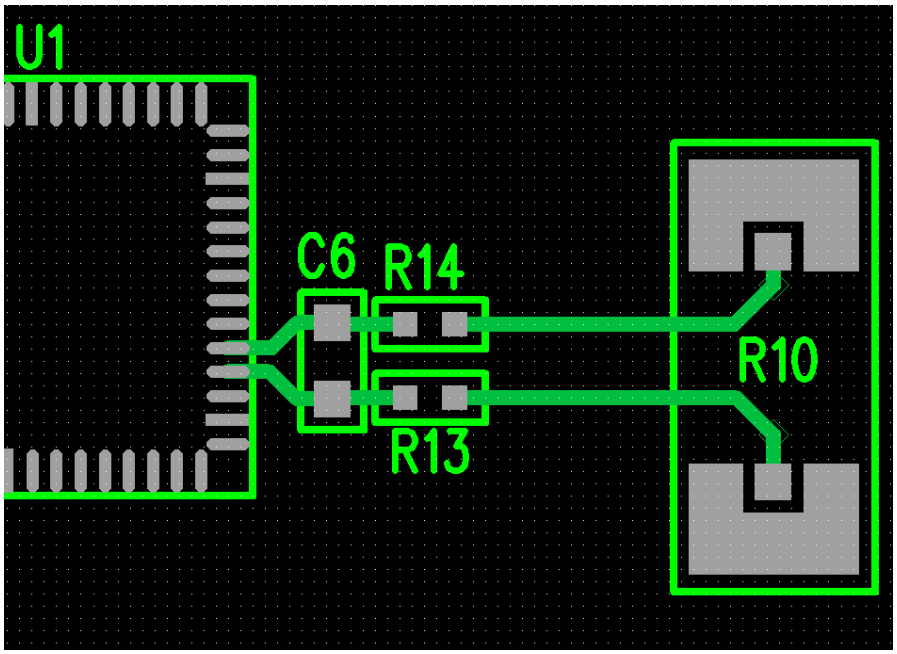

Illustration 2: Filter Placement

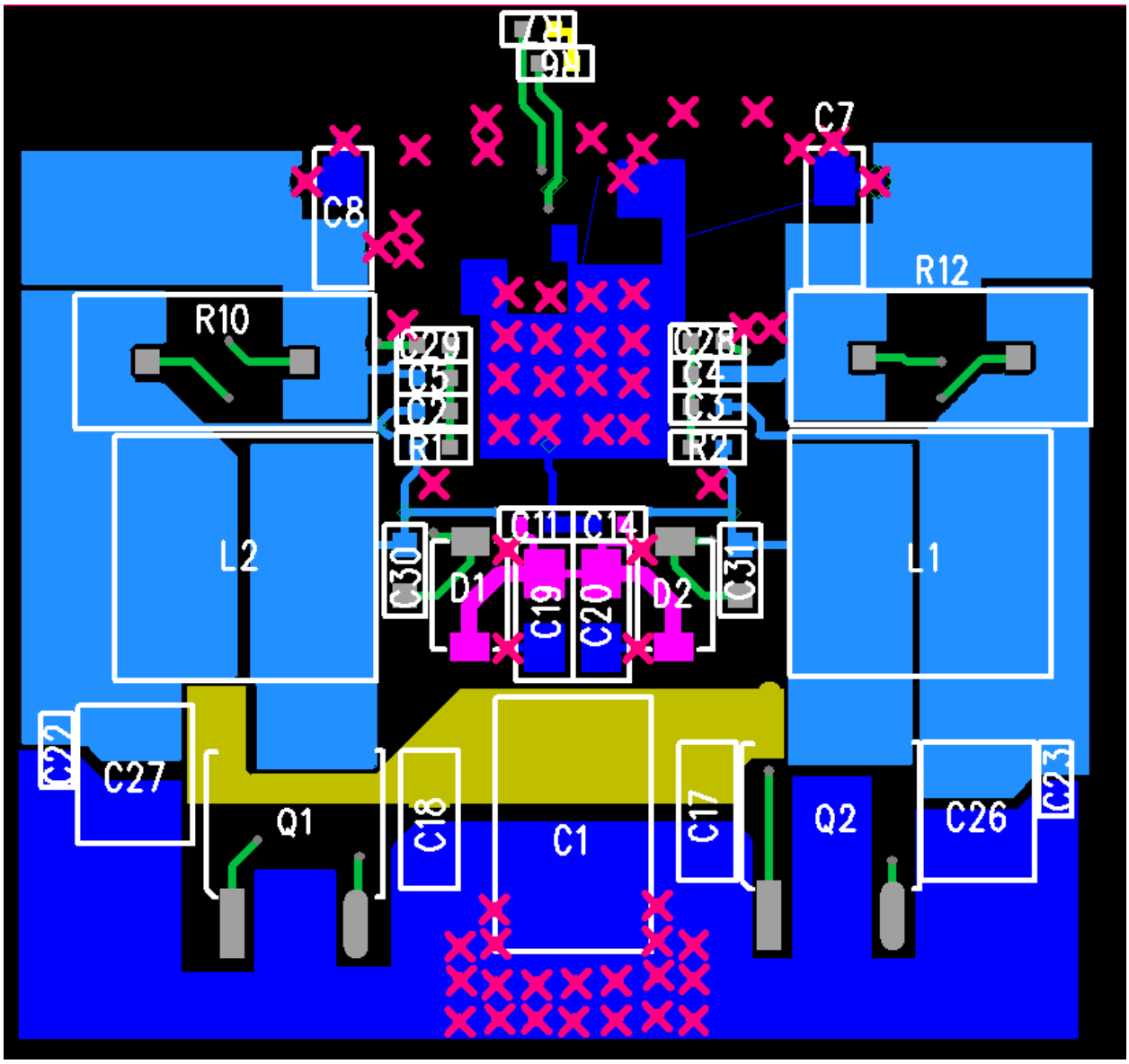

Illustration 3: Power Side

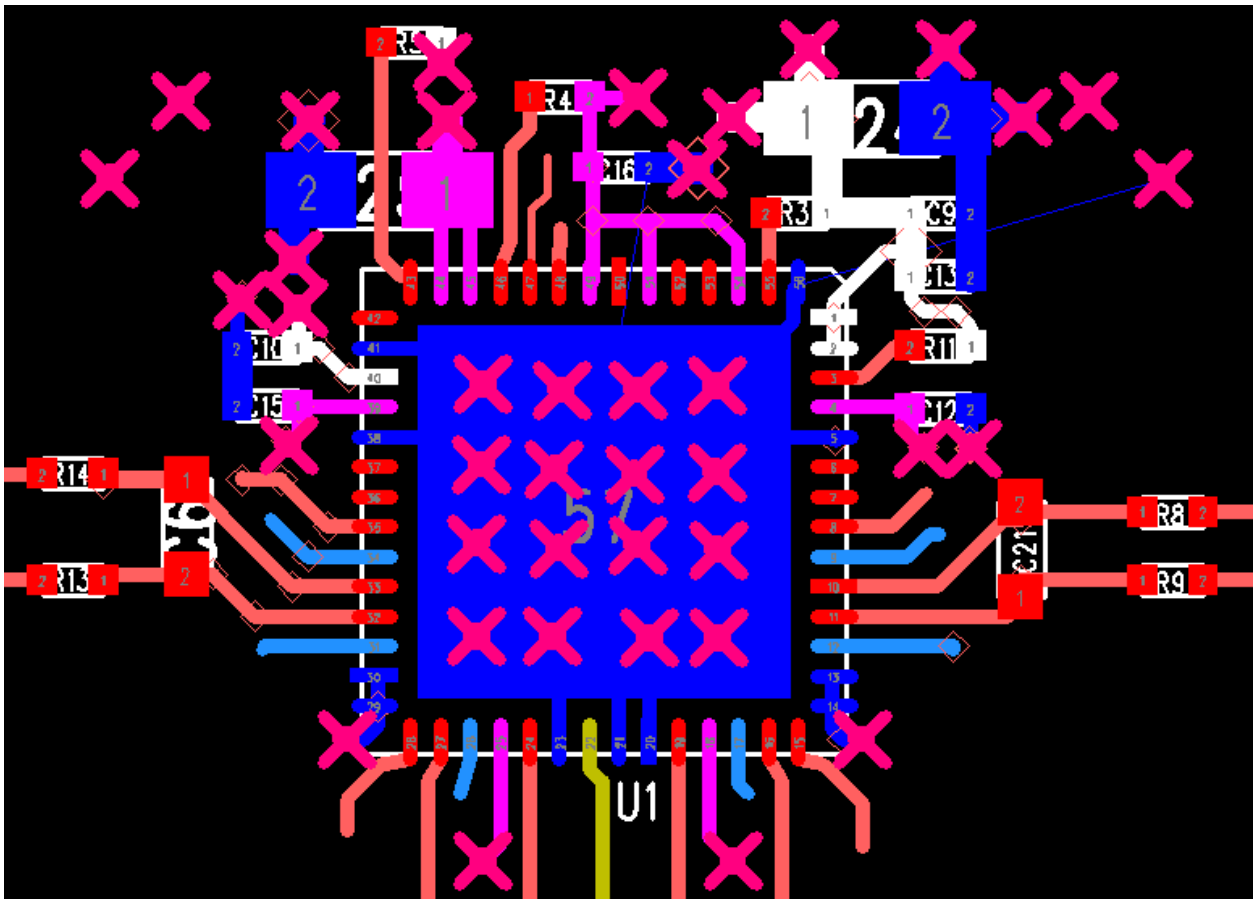

Illustration 4: PSG5220 Side

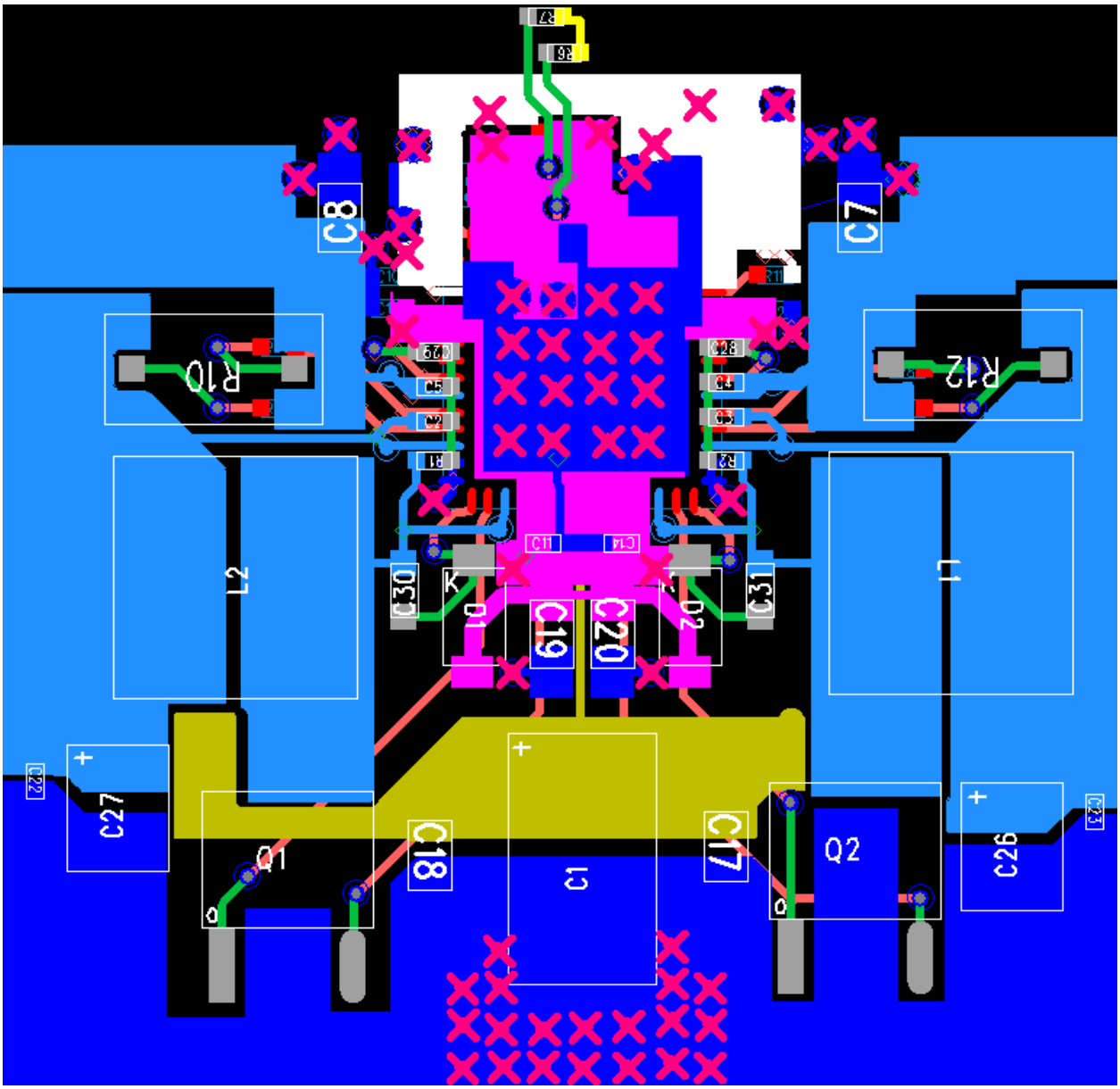

Illustration 5: Reference Layout

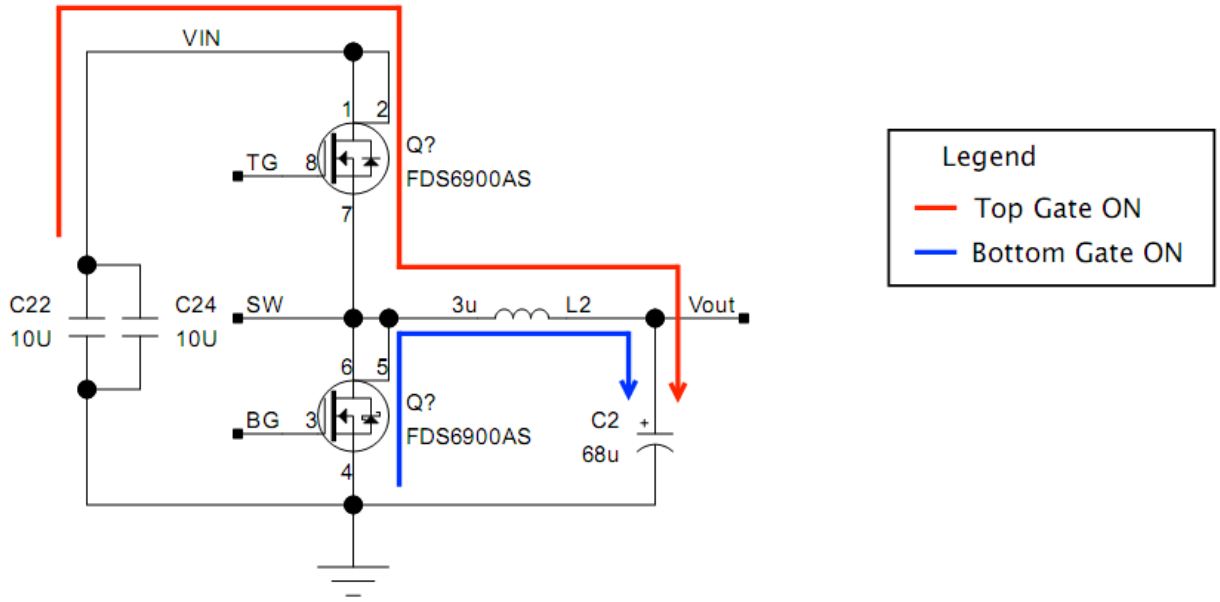

Illustration 6: Power Path