WHITE PAPER

Ultra-Low Noise Figure, High Gain Amplifier with High Linearity

Introduction

Infrastructure receiver applications for cellular/3G, ISM, GPS, WiMAX/4G, automotive applications, and satellite radio require Low-Noise Amplifiers (LNAs) with very low Noise Figures (NF), good input and output return loss, high linearity, low current, wide band stability, and robust performance. These conflicting design requirements are equally important, so they have to be achieved simultaneously. These challenging requirements demand highest available performance from the technology. To obtain an optimized performance with minimum trade-offs, unique design techniques and superior pHEMT process technology are used.

This White Paper describes different trade-offs, design options, and implementation of a sub 1 dB low NF (~ 0.6 dB), high gain (> 20 dB), and very high linearity (> +34 dBm) two-stage LNA.

The SKY65040-360LF LNA maintains a very low NF up to 2.5 GHz and an excellent 3rd Order Output Intercept Point (OIP3). The design is fabricated using Skyworks proprietary low-noise, high linearity depletion-mode pHEMT process. It is an ideal building block for base stations and satellite radios where NF and linearity (IIP3) are very critical. Typical applications include GSM, PCS, WCDMA, TD-SCDMA base stations, GPS and satellite radios.

LNA Topology and Technology

Design Requirements

The critical LNA design requirements for a representative base station receiver application are shown in Table 1. This sub 1 dB LNA is designed specifically for WCDMA base station applications. Therefore, the 3rd order intercept point (IP3) and 1 dB compression point (P1dB) requirements for this LNA are also very critical [1]. The usual technique of designing for low NF and power gain, and later tuning the design for good linearity, may not result in the optimum design trade-offs.

Output Return Loss (ORL) is given as the only parameter that has a secondary importance and can be traded off for better IP3.

Design Architecture

Low noise operation of an amplifier requires the bias current to be chosen around 15 to 25 percent of the drain source current (I_{DSS}) with the gate source voltage (V_{GS}) = 0. However, high linearity operation requires the bias current to be around 70 to 80 percent of I_{DSS}. The low NF and very high IP3 specifications dictate using about 20 percent of I_{DSS} for the first stage and the remaining current used for the second stage to achieve a high IP3.

With a cascaded design, first and second stages can be biased at different conditions. Individual voltage and current adjustment of each stage provides extra flexibility needed for further optimization. Gain and IP3 of the first or second stage can also be adjusted independently with minimum effect on NF. Therefore, a two stage LNA topology with cascaded common-source amplifying stages seems to provide the most flexibility and, therefore, optimum design trade offs.

Table 1. Two-Stage LNA Room Temperature-Critical Target Specifications at V_{DD} = 5 V and Operating Temperature = 25 °C

Parameter	Symbol	Target	Units of Measurement
Noise Figure	NF	0.6	dB
Gain	G_A	22	dB
Input return loss	IRL	15	dB
Output return loss	ORL	15	dB
Output 1 dB compression point	OP1dB	+18	dBm
3rd Order Output Intercept Point	OIP3	+34	dBm
Supply current	I_{DD}	60	mA

Table 2. Initial System Budget Calculations for NF and OIP3

Stage Data	Stage 1	Stage 2	Units of Measurement
Noise Figure	0.5	2.0	dB
Gain	13	9	dB
3rd Order Output Intercept Point	+30	+36	dBm
Supply current	22	40	mA

System	Stage 1	Stage 2	Units of Measurement
Noise Figure	0.6	–	dB
Gain	22	–	dB
3rd Order Output Intercept Point	+34.2	–	dBm

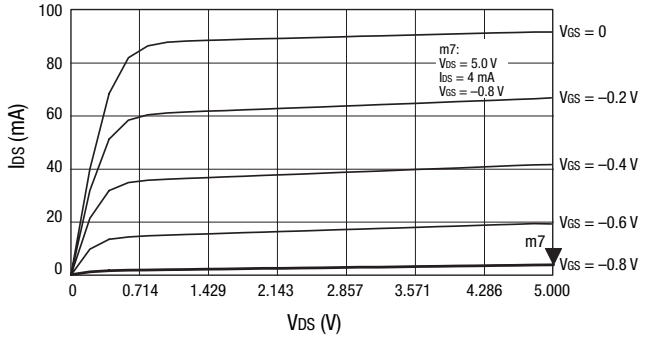

Figure 1. IV Curves of 300 μm Device

The IP3 can be further improved by presenting different impedance terminations to the device [2]. When more current is available, the second stage drain current can always be increased to improve IP3 and P1dB with a minimal impact on other performance parameters.

The initial cascaded analysis of a two-stage LNA is shown in Table 2. A good system budget analysis helps optimize the design and eliminates early mistakes. Higher gain for the first stage reduces the effect of the second stage in the overall NF and provides most of the necessary gain.

Process Technology and Biasing

This design uses Skyworks depletion mode, Low Noise Field Effect Transistor (LNFET) with a Thin Film Resistor (TFR) process. The LNFET/TFR 0.5 μm gate length process is specifically designed for superior low noise performance in high linearity applications. Accurate, proprietary models enable effective circuit design simulations.

To understand various trade-offs in biasing considerations, a 300 μm size device is used as a test vehicle for the first stage. Simulations were run using the Agilent ADS simulation tool. The IV curves of a 300 μm device are shown in Figure 1.

The graph in Figure 2 shows the maximum available gain versus drain current and voltages. The gain drops rapidly as the drain current goes below 20 mA (drain source voltage, V_{DS}= ~ –0.6 V, 20 percent of I_{DSS}). These plots also show that the gain stays about constant from V_{DS} = 2 to 5 V. Figure 3 shows minimum NF versus V_{DS} with varying V_{GS}.

Due to the nature of depletion mode technology, biasing the FET for optimum operation requires negative gate-to-source voltage. The current at the device saturating region is given by the following equation:

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where V_{GS} and V_P (pinch-off voltage) values are both negative.

A drain current of 20 mA corresponds to about –0.42 V of V_{GS} voltage. A self biasing network that eliminates a negative supply at the gate terminal is designed for optimum operation as shown in Figure 4. With this biasing technique, a resistor at the source (R_S) is used to set the positive source DC voltage and drain current. A large value bypass capacitor is needed to bypass R_S.

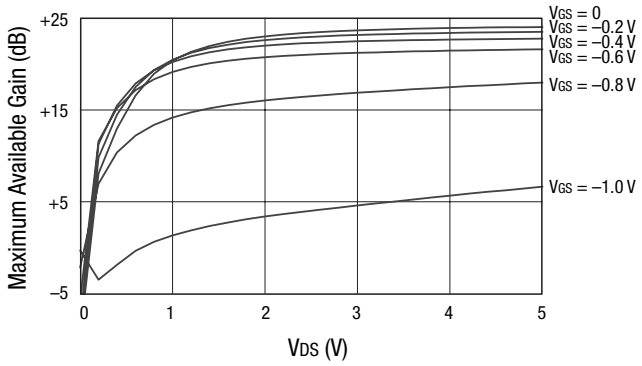

Figure 2. Maximum Available Gain vs V_{GS} (Current) at Varying V_{DS} for a 300 µm Device

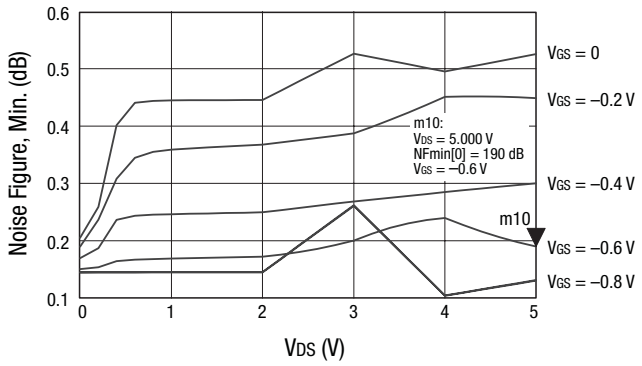

Figure 3. Minimum NF vs V_{GS} and V_{DS} for a 300 µm Device

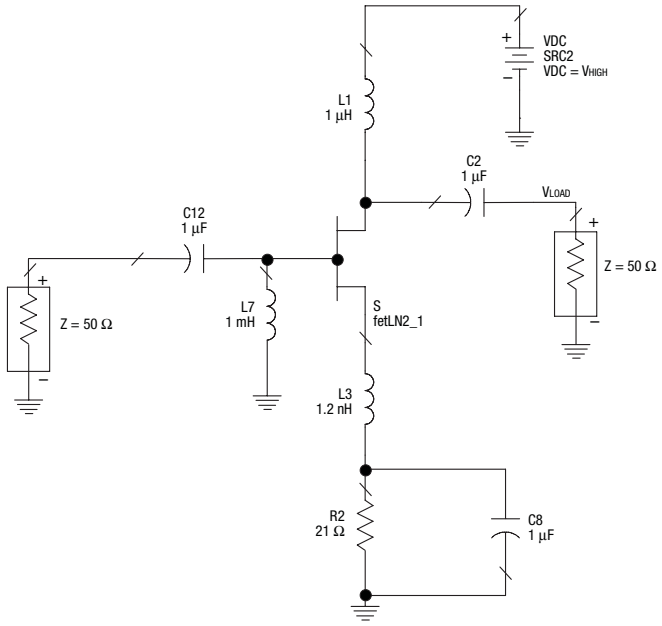

Figure 4. Amplifier Schematic Showing the FET Self-Bias Circuit

A simple method of a shunt inductor (or a very large value of shunt resistor) at the gate can be used for gate DC biasing. This inductor can also be used as part of the input matching network. A source resistor value of 21 Ω allows a V_{GS} voltage drop of –0.42 V between the gate and source terminals as shown in Figure 4.

Figure 5 shows available gain and noise circles on a Smith chart for a single stage design. The graph shows that gain starts to trade off with the NF if higher gain is desired from a single stage. Also, in a two-stage design as the gain of the first stage increases, IP3 and P1dB start to degrade due to earlier saturation of the second stage. Therefore, optimum trade-off between the gain, NF, and P1dB should be selected for the first stage. The system budget calculation shown in Table 2 allocates about 13 dB of gain for the first stage and 9 dB of gain for the second stage with a 2 dB gain margin allocated for the other circuit losses.

However, the second stage is mainly designed for P1dB and IP3 performance. Higher current provides higher OIP3 but the maximum total current specification of 60 mA forces allocation of about 45 mA to the second stage.

Design for Optimum NF and Input Match

Two of the design constraints, NF and input return loss, are the main factors used to determine the first stage design. Based on the design considerations discussed earlier, the total device periphery of 300 µm is chosen for the first stage. This was mainly done to provide broadband gain performance with low current

operation at the same time. The I_{DSS} for this device is around 90 mA.

The device is biased at 20 mA current for optimum NF and gain trade off. The target for total NF shown in Table 2 is 0.6 dB. System analysis shows that the NF has to be below 0.5 dB for the first stage. The bare FET device provides a minimum NF of about 0.3 dB. This leaves about 0.2 dB of NF degradation for all other factors.

About 0.05 dB of loss can be allocated to the resistive losses due to the bias circuitry at 2 GHz and source inductor resistive losses. This allows for about 0.15 dB of resistive loss for the input match, assuming that the input is matched for the optimum NF impedance.

To meet 0.15 dB of input match resistive loss at 2 GHz, Agilent ADS simulations show that quality factors > 60 for inductors, and > 200 for capacitors are needed.

The inductive degeneration technique is used for simultaneously optimizing NF and input match.

Design for Linearity (IP3) and P1dB

As mentioned earlier, P1dB and IP3 determine the second stage design. The measured device data available was at an input power (P_{IN}) = –18 dBm. However, the system gain allocations show that a P_{IN} ~ –5 dBm is present at the input of the second stage device. Therefore, simulation models are used to estimate OIP3 at P_{IN} = –5 dBm.

The OIP3 and P1dB simulations were performed using 50 Ω input and output impedance conditions at 2 GHz. Figure 6 shows P1dB and OIP3 contours. Simulations show around +18 dBm P1dB and +33 dBm OIP3 are achievable. Since the OIP3 requirement is higher than what 50 Ω source and load conditions provide, source and load matching needs to be done to improve OIP3.

Input and output terminations in band and out of band directly affect the linearity performance of the amplifier. The input and output terminations of the amplifier can be swept directly through source and load pull techniques. The Agilent ADS large signal source and load pull setup are shown in Figure 7.

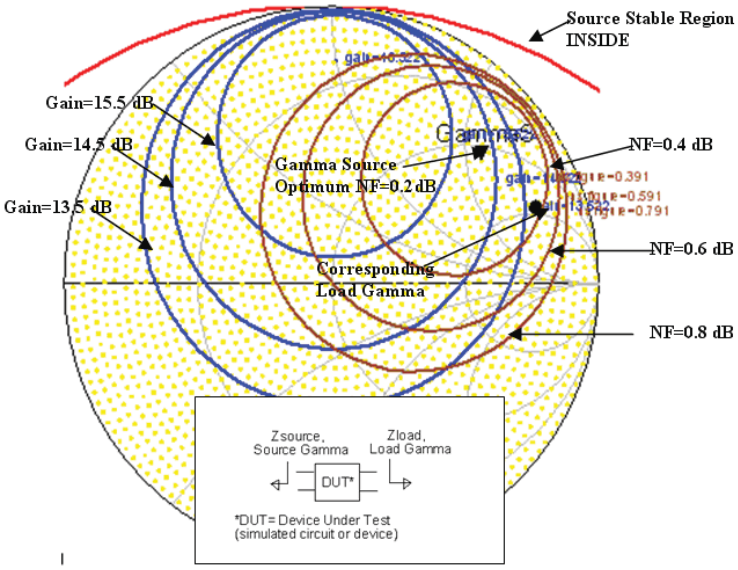

Figure 5. Available Gain and Noise Circles

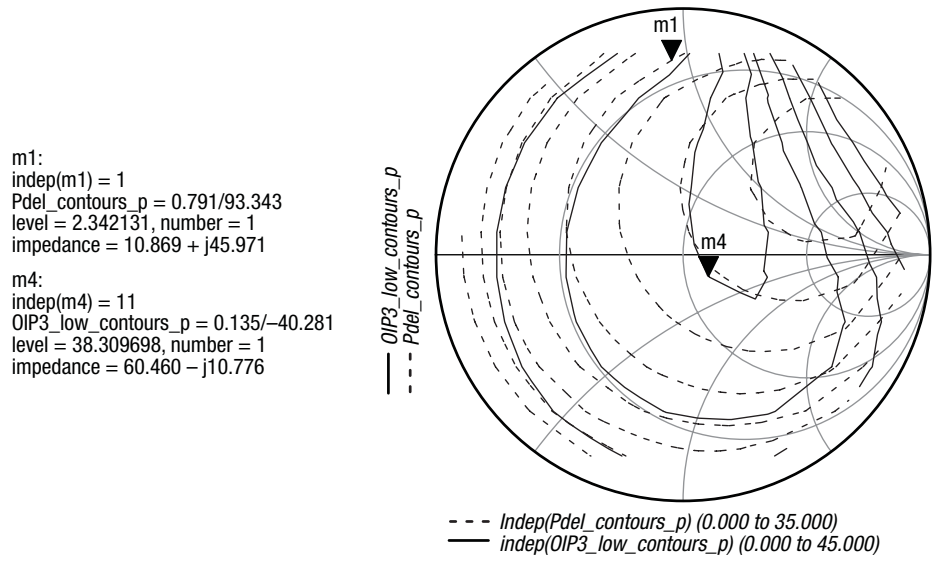

Figure 6. OIP3 and Delivered Power Contours

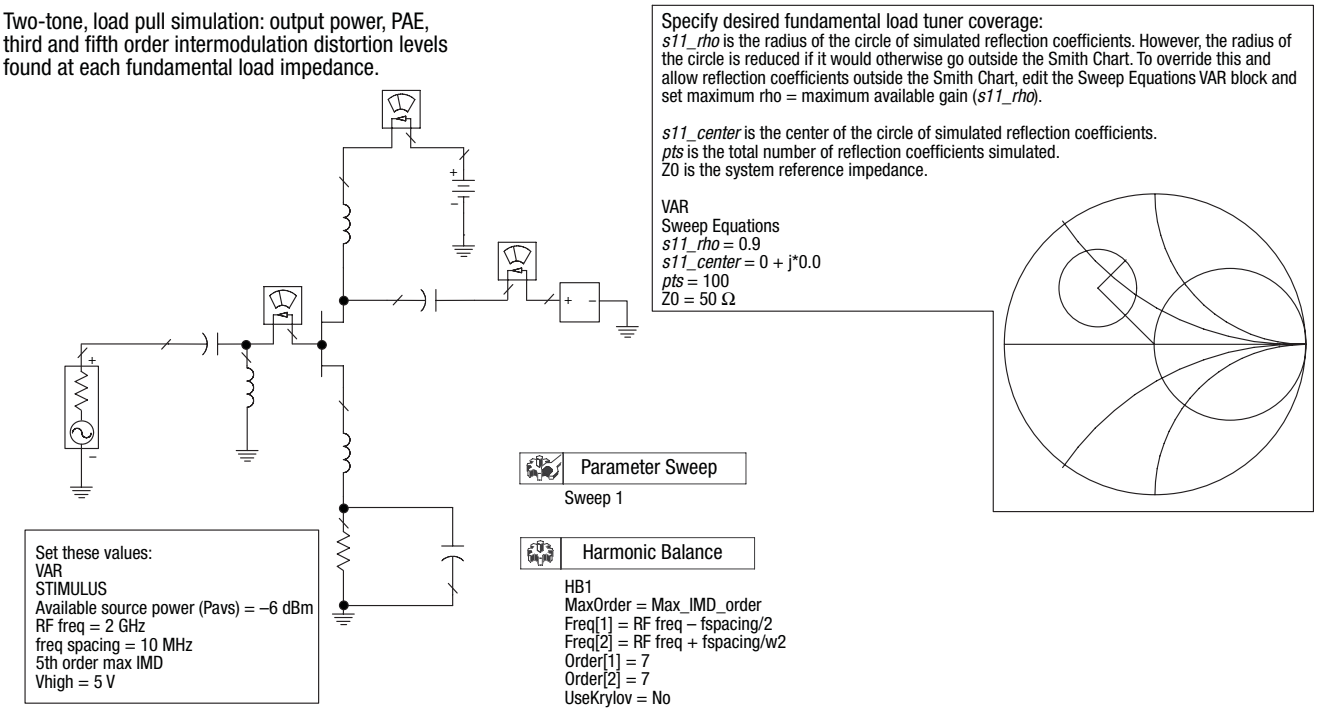

Figure 7. Agilent ADS Large Signal Source and Load Pull Test Setup for a Common Source pHEMT Amplifier

The inter-stage matching network determines the IP3 input source termination for the second stage. To determine the optimum impedance for best OIP3, a source and load pull is performed independently. Impedance points are shown in Figure 6.

Load pull results show that with a 50 Ω source impedance, the maximum OIP3 that can be achieved is +35.7 dBm. Source pull results with a 50 Ω load impedance show that a maximum OIP3 of +39 dBm can be achieved. Based on this data, a source impedance point of $Z_S = 20 + j60\ \Omega$ that provides an OIP3 of about +37 dBm OIP3 is chosen. After the source is matched, load pull is performed again. Figures 8 and 9 show P1dB and OIP3 results, respectively, after the source is matched.

Simulations show that a maximum OIP3 of around +43 dBm can be achieved after source and load pull when both are matched for best OIP3. When this is designed as the second stage of a cascaded amplifier, the input match serves as a matching circuit between the first and the second stage. Final load pull simulation and matching should be done after connecting the two stages together.

Design For Stability

Stability is one of the most important requirements to consider for an LNA. Typical specifications dictate unconditionally stable operation up to 18 GHz. Each stage must be designed for unconditionally stable operation as well as the total two stage design that includes all the external components and biasing over all conditions.

A very low noise device with high gain usually becomes highly unstable in most of the frequency range. To stabilize the device and meet these requirements, multiple stability design techniques have been used. To solve stability problems at low to higher operating frequencies, some value of a source inductor is generally used.

A source degeneration inductor is used for input; a NF match can be used for this purpose as well. One technique that is commonly used is to have a series-parallel LR network. This network behaves like a low impedance at low frequencies and a high impedance at higher frequencies. Another technique that is commonly used is a shunt-series CR network connected from drain to ground. This network behaves like a shunt resistor at high frequencies and high impedance at low frequencies. A shunt resistor connected to ground helps to stabilize the device.

Another method that is used to improve stability is the shunt feedback between the output and the input of the device. However, this method degrades the NF. Therefore, it is not used in the first stage design but is used in the second stage design. This feedback also helps the IP3, return loss, and gain adjustment.

Figures 10 and 11 show stability results before and after these stability techniques are used, respectively. Figure 10 shows that the design is stable only within a small frequency band. After using the stabilizing circuits, the design becomes unconditionally stable from 0.05 to 18 GHz as shown in Figure 11. Stabilizing circuits are integrated into the two-stage cascaded LNA. Final simulation and measurement results are presented in the following section.

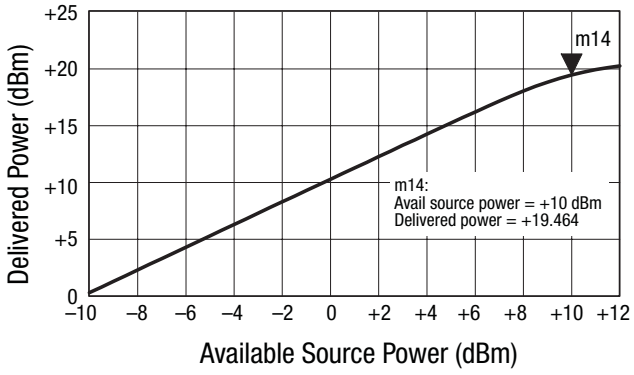

Figure 8. P1dB After Source is Matched

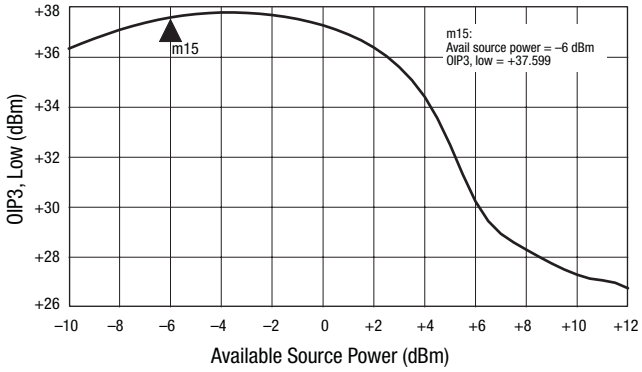

Figure 9. OIP3 After Source is Matched

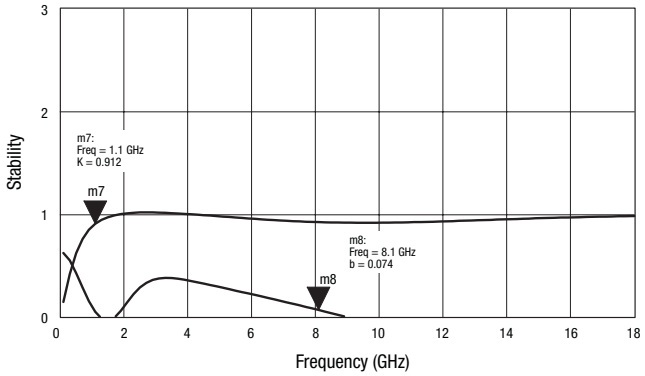

Figure 10. Before Stability Fixing Circuit Added

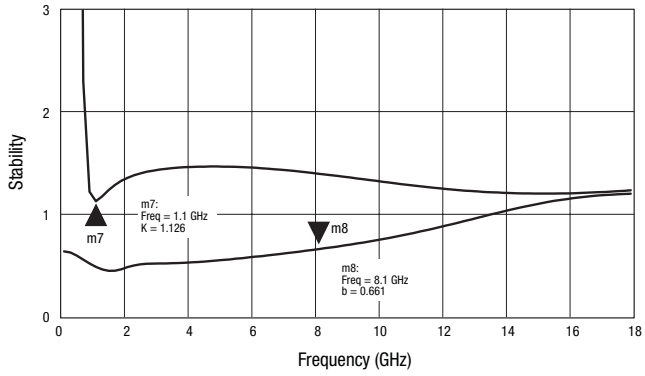

Figure 11. After Stability Fixing Circuit Added

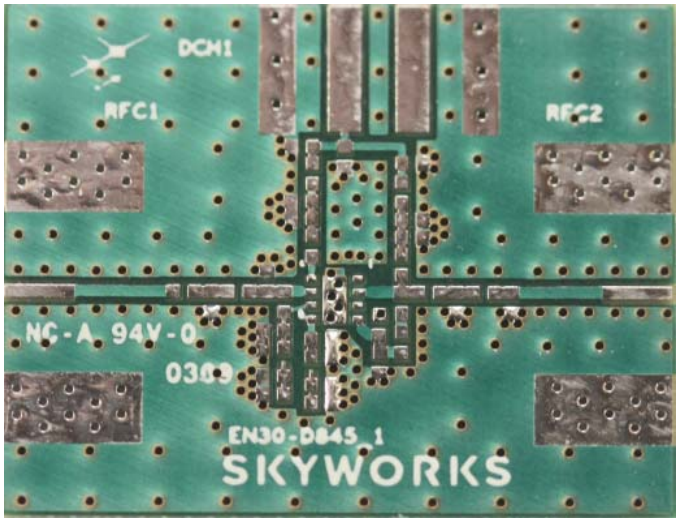

Figure 12. Bare Test Board

Test Board Layout and Grounding

A good test board design is important to achieve the expected performance. Special attention must be given to minimize unwanted parasitics and to ensure proper grounding. Grounding is particularly important to simultaneously ensure high gain and unconditional stability.

As can be seen in Figure 12, a grounded Coplanar Waveguide (CPW) transmission line was used for component tuning flexibility and provides signal isolation due to its top ground metal. The test board was realized on an FR4 VT-47 (0.254 mm thick) for its lower loss, cost, and reasonably low dielectric constant.

An automated board assembly requires minimum spacing rules to be followed. Selecting a very high dielectric constant material may make the circuit very small but it can also turn design rule spacings into undesired phase shifts. The line width and spacing to the ground plane were selected to fit shunt 0402 sized surface mount components while maintaining a uniform 50 Ω line even when shunt components are not populated.

Vias are used on each side of CPW lines to reach the bottom common ground plane. Vias are inductive and their inductance is a factor of their aspect ratio. Although vias having a bigger diameter for a fixed length are less inductive and therefore preferred, their size may prevent placement in required locations.

As frequency increases, vias become increasingly inductive. This may result in an RF feedback path through the top ground metal, leading to instabilities. For that reason, the top ground plane is intentionally broken in various sections to open any potential RF current feedback loops. The remaining metal islands are grounded to avoid creating unwanted resonators. More vias are used along the metal edges for improved high frequency performance.

Vias should also be placed as close as possible to board components to minimize the electrical length to the ground

reference, which includes the vias' length. Although electrical lengths may be very small in the band of operation, they can be a source of important phase shifts at high frequencies. The most ground-sensitive regions to achieve good performance of the LNA are the input matching circuit and the RF decoupling regions of the drain and source terminals of each stage. Both of these important areas are addressed in the Evaluation Board design by adding vias to minimize parasitic inductance.

Component Selection Considerations

Component selection is affected by various factors such as component parasitics, the component location in the circuit, the frequency range of operation, and the intended purpose for the component.

Figure 13 shows the test board circuit schematic. A feedback circuit can be used if gain adjustment is needed. In that case, components C15 and C16 are typically populated with a capacitor and a resistor, respectively.

The input and noise matching network is composed of components C1, L1, and L2. As any source of loss at the input of an LNA directly contributes to its NF, the components used at the input must have a reasonably high quality factor. Output match is achieved by components C10, L5, and L6.

Out of band oscillations are addressed by additional capacitors C8 and C9 to decouple lower frequencies traveling through the choke inductors at both stages. Capacitors C2, C3, and C13 decouple the highest frequencies up to 18 GHz. The placement of these capacitors is critical to avoid instability at these frequencies. Resistors R3 and R4 also contribute to stability as they present a higher resistance to RF from output to input of the device.

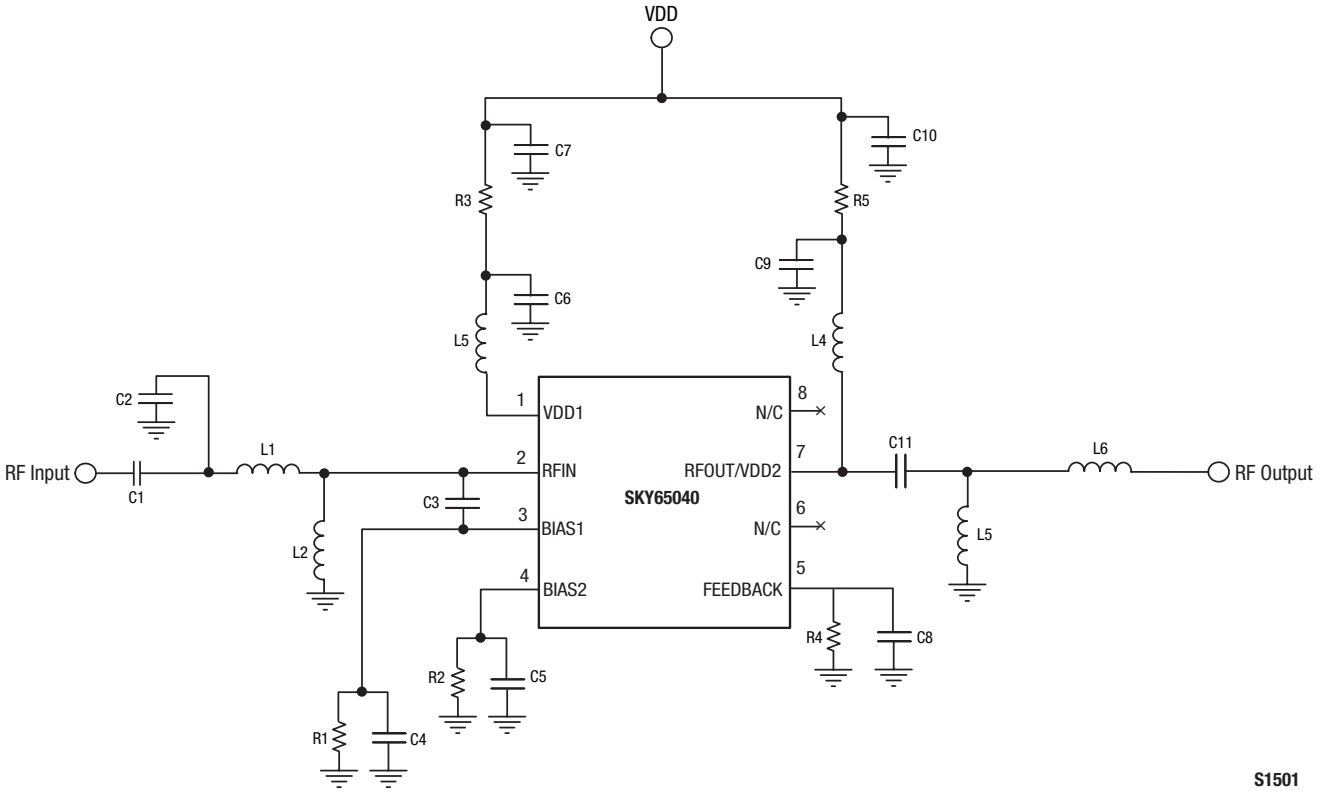

Figure 13. Evaluation Board Schematic

Measured vs Simulated Results

A manufactured amplifier was tested on the test board at a supply voltage (V_{DD}) of 5 V. This voltage sets a bias point at the first stage as V_{DS} = 2.4 V at a drain voltage (I_D) = 23 mA, and a bias point at the second stage as V_{DS} = 4.2 V at I_D = 46 mA.

Figure 14 shows measured and simulated NFs in a bandwidth of 1.92 to 1.98 GHz. The loss of the input transmission line was measured as 0.1 dB in this band. The NF is measured as 0.65 dB at 1.95 GHz after de-embedding the input transmission line loss.

Figure 15 shows simulated and measured two-stage amplifier gain as functions of frequency. The gain is 24.8 dB at 1.95 GHz. The inset in Figure 15 below is a narrow-band view of the gain within the frequency band.

Figures 16 and 17 show simulated and measured input return loss and output return loss, respectively. Both input and output return loss measure greater than 20 dB in the passband.

Figure 18 shows measured OIP3 within the band. The input power of –18 dBm per tone was applied at two fundamental frequencies of 1947.5 and 1952.5 MHz.

Figure 19 shows input power at the 1 dB input compression point (IP1dB), measured at –7.2 dBm. The output power at the 1 dB output compression point (OP1dB) is measured at +17.6 dBm.

Conclusion

Many performance aspects must be considered in the design of LNAs. Next generation LNAs require new technologies and design techniques to meet the increasing demands of the market. An optimized design with proprietary pHEMT technology discussed in this White Paper will be required to meet the challenging performance requirements of new products while keeping the cost low and maintaining small size.

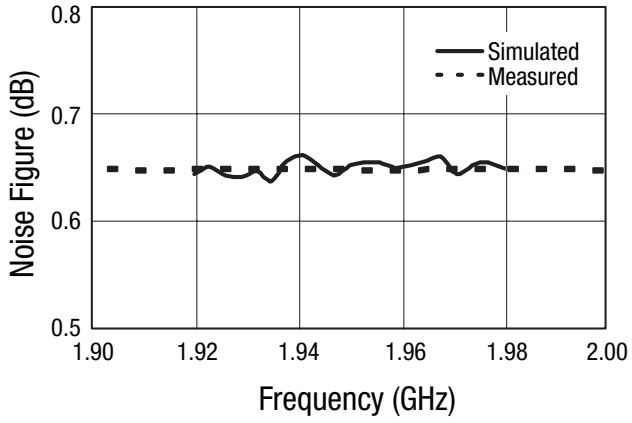

Figure 14. Simulated and Measured Noise Figure

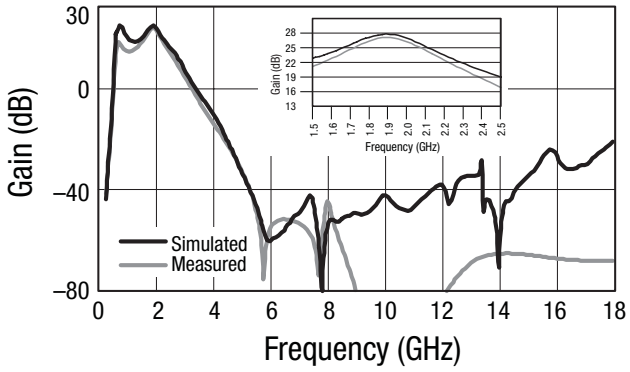

Figure 15. Simulated and Measured Gain

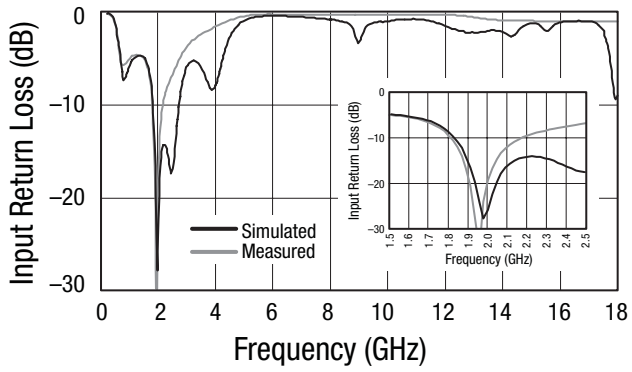

Figure 16. Simulated and Measured Input Return Losses

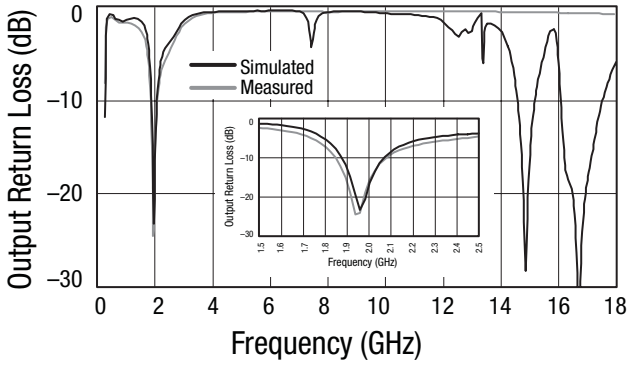

Figure 17. Simulated and Measured Output Return Losses

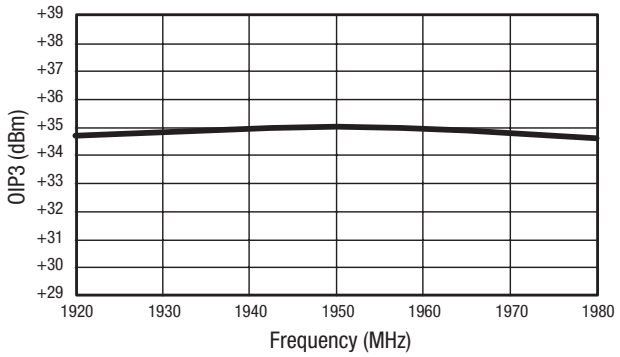

Figure 18. Measured Output 3rd Order Intercept Point

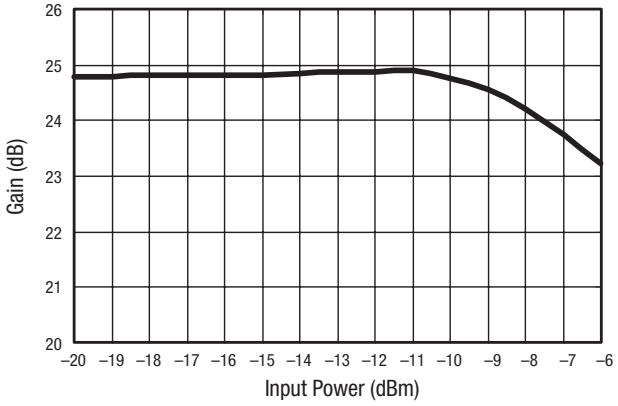

Figure 19. Measured Input Power at 1 dB Compression Point

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2. Maas, Stephen A., *Nonlinear Microwave Circuits*, IEEE Press, pp. 349-351.