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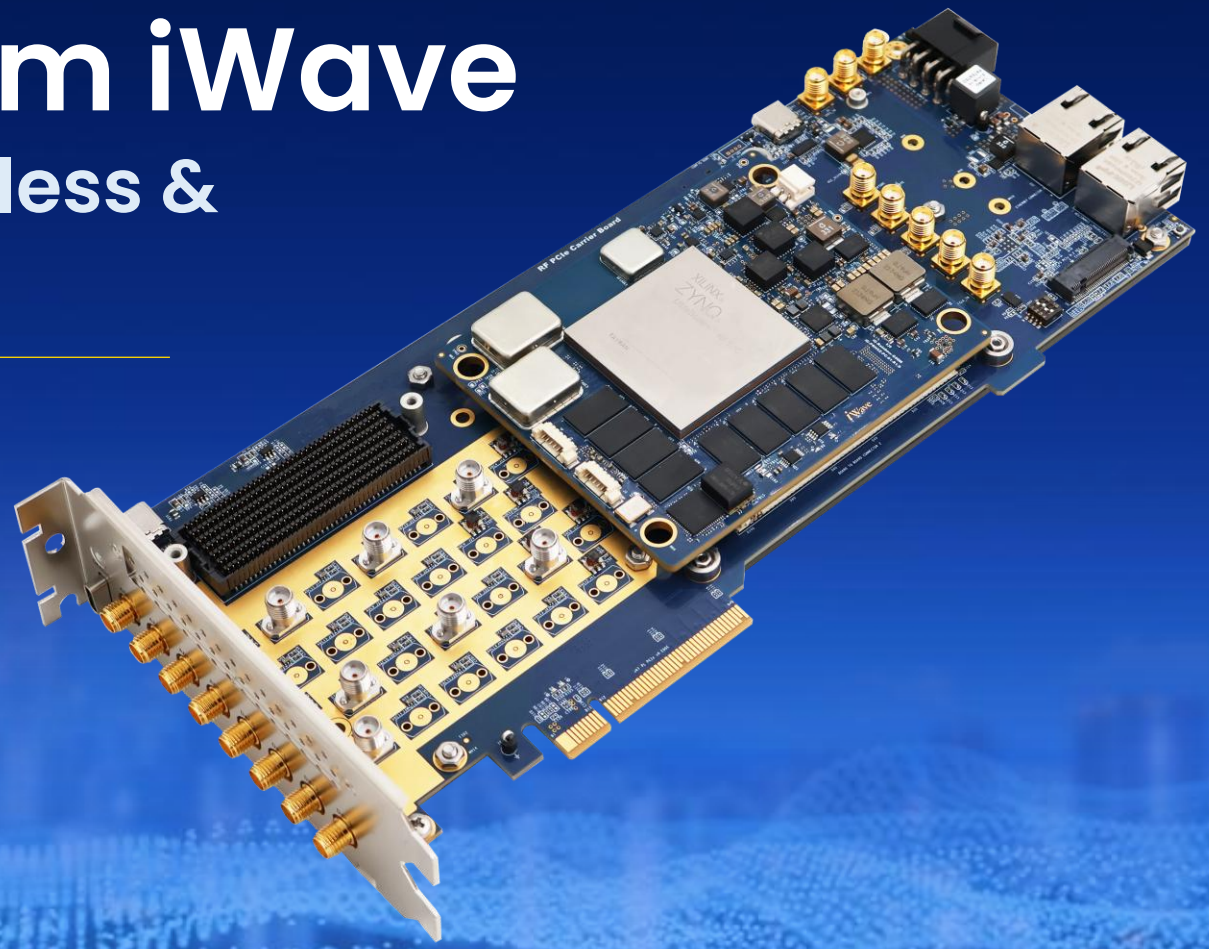
eBook

RFSoC Solutions from iWave

Powering SDR, EW, Radar, Wireless & Computing Solutions

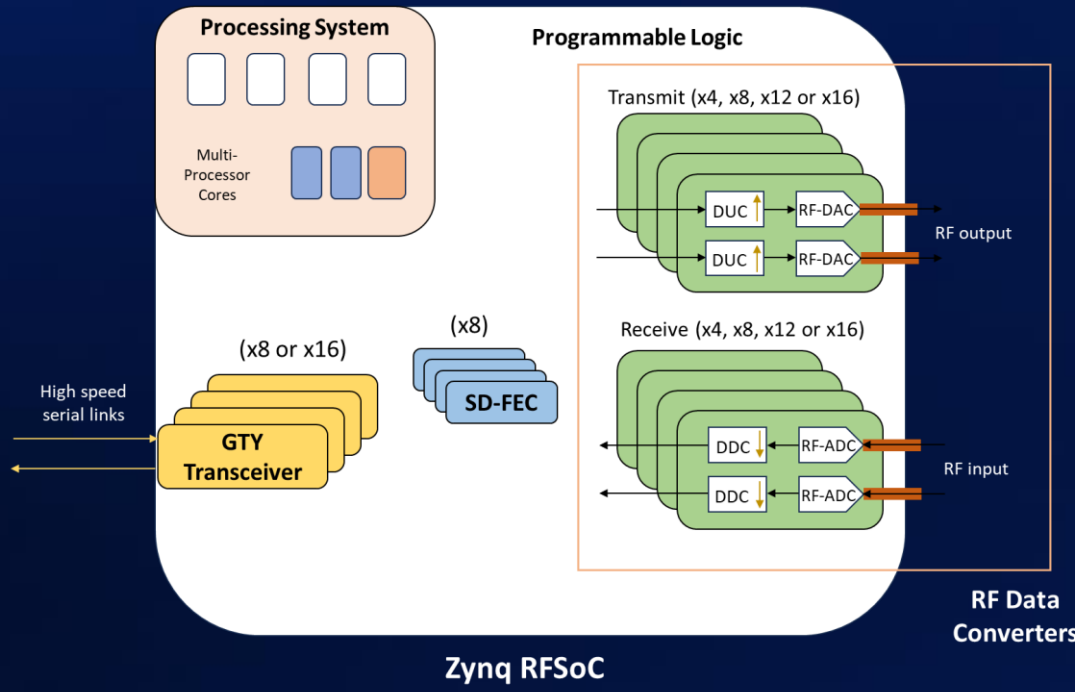


What is RFSoC?

The Zynq™ UltraScale+™ RFSoC is a heterogeneous compute architecture that includes a full Arm processing subsystem, FPGA fabric, and complete analog/digital programmability across the RF signal chain.

This monolithic integration streamlines design complexity and enhances performance, making it ideal for applications where size, power, and throughput are critical

The SoC provides a complete, single chip software-defined radio platform for diverse applications, and the ability to produce radio variants as market dynamics evolve.



Why Zynq™ UltraScale+™ RFSoC?

- Integration of RF Analog
- High-speed ADCs and DACs with built-in front-end signal conditioning and optimized hardened DSP blocks
- Integrated high-speed transceivers supporting multi-gigabit serial communication over standard interfaces
- Dedicated hardened IP blocks for Forward Error Correction (FEC)

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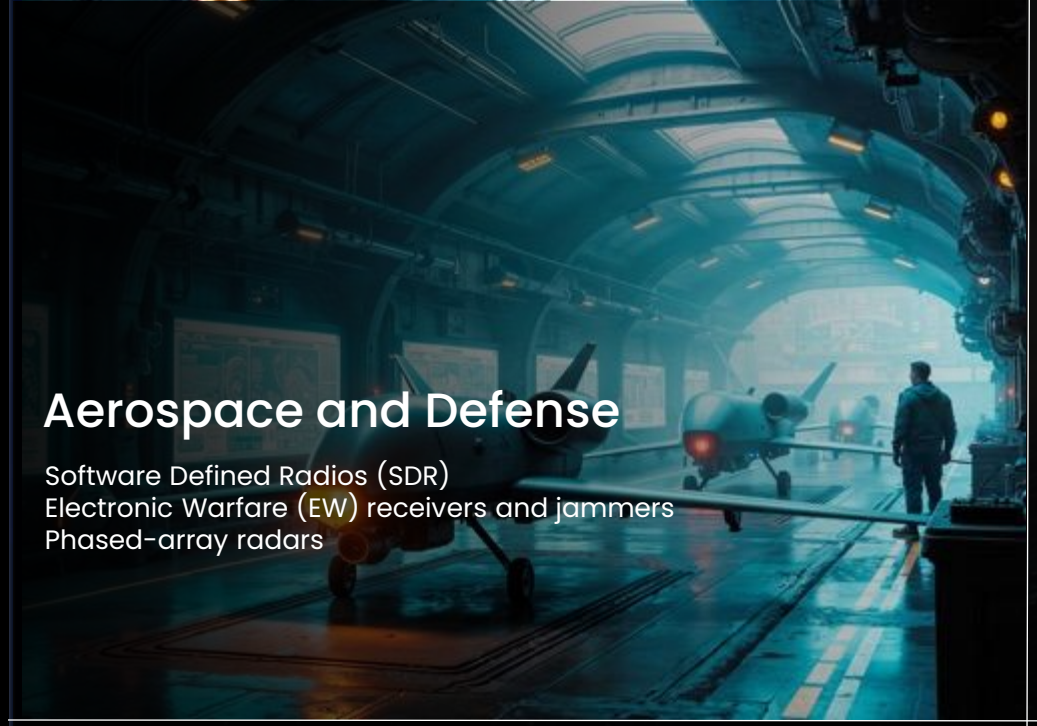
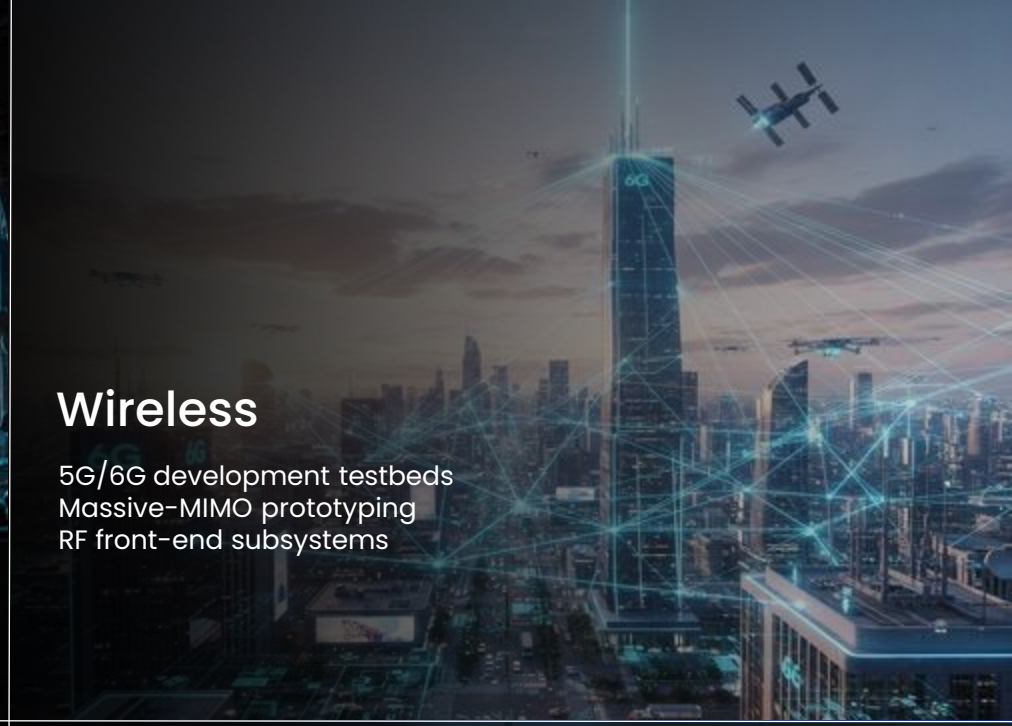
RFSoC Applications



Aerospace and Defense

Software Defined Radios (SDR)
Electronic Warfare (EW) receivers and jammers
Phased-array radars



Wireless

5G/6G development testbeds
Massive-MIMO prototyping
RF front-end subsystems

Space and Satellite

Communication gateways
Wideband channelizers
Ground station RF processing

Industrial

High-speed data acquisition
RF instrumentation
Quantum computing control systems

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RFSoC System on Module

What & Why ?

Core Components

- Zynq™ UltraScale+™ RFSoC FPGA

Memory & Storage

- Up to 16GB DDR4 RAM for PS with ECC
- Up to 16GB DDR4 RAM for PL
- Up to 128GB eMMC Flash
- 256MB QSPI Flash and EEPROM

Connectivity

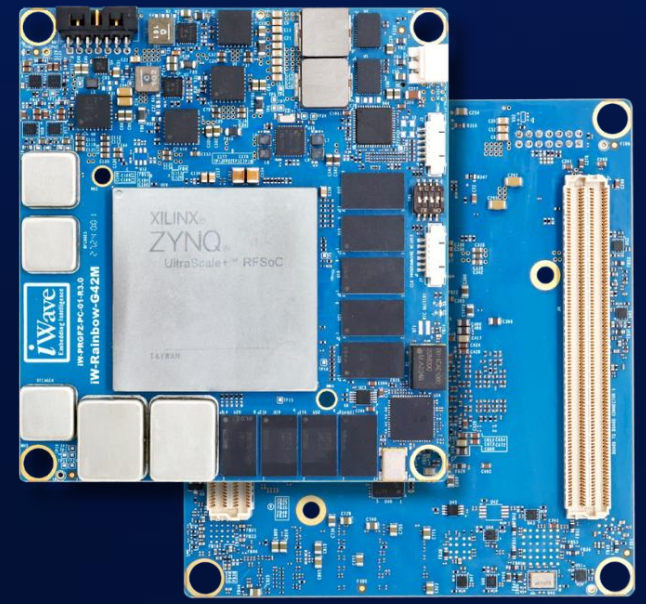
- 2 x 400 pin B2B Connectors
- 16 x PL GTY transceivers up to 28.21Gbps
- 4 x PS GTR transceivers up to 6Gbps
- Supports PCIe Gen3 x 8 / Gen4 x 16
- Gigabit Ethernet, CAN, SD

On-Module Clocking & Synchronization

- Analog SYSREF, PL-SYSREF, PL Clock for the synchronization
- Ultra-low-noise RF PLLs
- Network synchronizer clocks
- External 10MHz clock support for MTS

Power & Thermal

- Low-noise regulators for best RF performance
- Rugged Mechanical enclosure with thermal solution



Why consider RFSoC System on Module?

- SoM takes care of power sequencing, signal integrity, and high-speed layout reducing system design complexity
- Qualified and Validated Solution
- Accelerate your time to market with reduced risk
- Scalability and Modularity across Product Family
- Production Ready
- Product Lifecycle Management taken care by iWave

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RFSoC Boards & Solutions

System on Modules

An extensive portfolio of Sytem on Modules across the RFSoC product family ensuring the right product fit as per your requirements. The System on Modules are all pre-qualified, validated and production ready.

3U VPX and PCIe Cards

RFSoC based COTS modules for the aerospace, defense, networking and storage applications. The portfoilio of PCIe Cards and 3U VPX Cards are availabe across different FPGA variants.

Custom Design

iWave enables customers with custom carrier card and system design. iWave carries RF ODM expertise to enable your products from ideation to production.

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RFSoC Solutions Roadmap

Performance

SOM
ZU49/ZU39/ZU29DR

ADC & DAC
RFSoC PCIe Card
ZU49/ZU39/ZU29DR

3U VPX
ZU48/47/43/28/27/25DR

SOM
ZU48/47/43/28/27/25DR

ADC & DAC
RFSoC PCIe Card
ZU48/47/43/28/27/25DR

3U VPX
ZU49/ZU39/ZU29DR

3U VPX ✷
ZU67/65/64/63DR

ADC & DAC ✷
RFSoC PCIe Card
ZU67/65/64/63DR

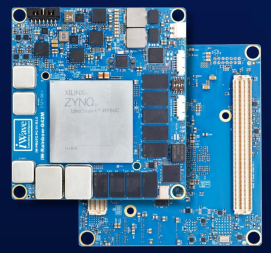
SOM
Versal™ RF ✷

ZU49DR-ML ✷

ZU67/65/64/63DR ✷

System on Module Portfolio

iG-G42M



ZU49/ZU39/ZU29DR

- 16 x ADC channels up to 2.5Gsps
- 16 x DAC channels up to 10Gsps

iG-G42M-ML

XQ - ZU49DR

- 8 x ADC channels up to 5Gsps
- 8 x DAC channels up to 10Gsps

iG-G60M

ZU48/47/43/28/27/25DR

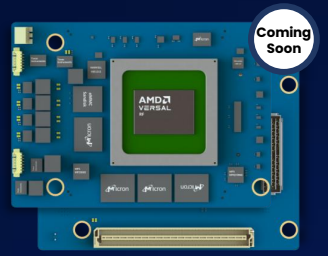
- 8 x ADC channels up to 5Gsps
- 8 x DAC channels up to 10Gsps

iG-G79M

ZU67/65/64/63DR

- 8 x ADC Channels up to 5.9Gsps
- 8 x DAC Channels up to 10Gsps

iG-G80M



Versal™ RF Series

- 16/8 ADC Channels up to 8/32Gsps
- 16 DAC Channel support up to 16Gsps

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Versal™ RF Series

COMING SOON

COMING SOON

COMING SOON

Processing System (PS)

- Dual® Arm® Cortex-A72 @1.65GHz
- Dual Arm Cortex-R5F @800MHz

Programming Logic (PL)

- Up to 2,473.8K Logic cells & 1,130.88K LUTs
- GTM2 High Speed Transceivers x 20 @112 Gbps

AI Engine (AIE)

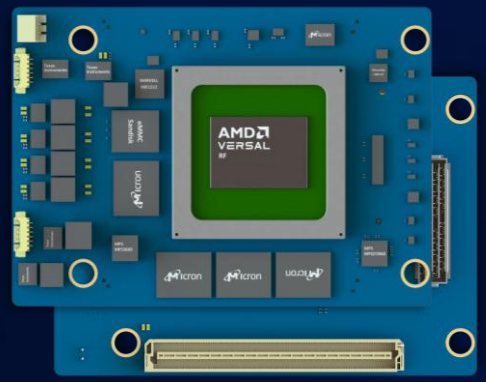
- AI Engine Tiles up to 126
- AI Data Memory up to 32Mb

High Performance Memory

- 32bit, 4GB LPDDR5X from PS
- 32bit, 4GB LPDDR5X from PL
- 2 x Dual Channel (2x16bit) 4GB
- LPDDR5X from PL

Storage

- 32GB eMMC Flash, 2Kb EEPROM
- 256MB (8bit) OSPI Flash or 256MB (4bit)
- QSPI flash from PS



FPGA

- Versal™ RF Family with VSVA2488 Package
- Compatible with VR1952/1902/1652/1602 devices

ADC / DAC

- 16/8 x ADC Channels up to 8/32Gsps
- 16 x DAC Channels up to 16Gsps

2 x 400pin Board to Board Connectors

- X5IO Bank IOs – up to 64LVDS/128SE
- HD Bank IOs – up to 11DIFF/22SE

High-Speed Transceivers

- PCIe x4 Gen5 through GTYP Transceivers
- 20/10 GTM2 High Speed Transceivers
- (Up to 56Gbps/112Gbps)
- or 12 GTYP High Speed Transceivers(Up to 32Gbps)

General

- Power Input: 12V through B2B Connector2
- BSP Support: Linux BSP: Yocto 2025.1 or higher

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Unique Features of RFSoC SOM from iWave

iWave extends AMD RFSoC capabilities with production-ready engineering features that reduce risk and accelerate deployment.

On-SOM Ultra-Low-Noise RF PLLs

- ✓ Clocking for ADC/DAC
- ✓ SYSREF and PL clocks
- ✓ 10MHz sync input for MTS
- ✓ Reduces carrier board RF complexity

On-SOM Network Synchronizer

- ✓ Reference clocks for PL & GTY
- ✓ Supports PTP & SyncE
- ✓ 1PPS IN/OUT for system-level sync

Ultra-Low-Noise Power Design

- ✓ Dedicated RF power rails
- ✓ Improved SFDR & SNR
- ✓ Better direct-RF sampling accuracy

MTS Support with Pin Compatible SOM

- ✓ Sub-100ps alignment
- ✓ Coherent sampling across multiple boards
- ✓ External 10MHz in clock support for synchronization

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PCIe Cards

iG-G42P

ZU49/ZU39/ZU29DR

- 16 x ADC channels up to 2.5Gsps
- 16 x DAC channels up to 10Gsps
- RF Length Match for iG-G42M ZU49DR (To support MTS) with iG-G42P carrier card

iG-G60P

ZU48/47/43/28/27/25DR

- 8 x ADC channels up to 5Gsps
- 8 x DAC channels up to 10Gsps
- RF Length Match for iG-G60M ZU48/47/43DR (To support MTS) with iG-G42P carrier card

iG-G79P

ZU67/ZU65/ZU64/ZU63DR

- 8 x ADC channels up to 5Gsps
- 8 x DAC channels up to 10Gsps
- Integrated DFE IP Block

PCIe ADC/DAC Cards for Quick Evaluation

Single carrier card enabling scalability across the family

Multi-tile, Multi board sync support

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RFSoC 3U VPX Card

SOSA
Sensor Open Systems Architecture

iG-G42V

ZU49/ZU39/ZU29DR

- 16 x ADC channels | up to 2.5Gsps
- 16 x DAC channels | up to 10Gsps

iG-G60V

ZU48/47/43/28/27/25DR

- 8 DAC channels | 30 MHz–6 GHz | up to 9.85Gsps
- 8 ADC channels | 30 MHz–6 GHz | up to 5Gsps

iG-G79V

ZU67/ZU65/ZU64/ZU63DR

- 8 x ADC channels | up to 2.95Gsps and 2 x ADC channels | up to 5.9Gsps
- 8 x DAC channels | up to 10Gsps

VITA 67.3 NanoRF Optical Hybrid Ferrule with 10 RF Channels and 100G Optical

Module Profile : MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-n

Slot Profile : SLT3p-PAY-1F1U1S1S1U1U4F1J-14.6.13-n

Also Supports other SLT3 slot profiles

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RF Expertise

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Comprehensive RF System Design

- Expertise in designing high-speed, high-density Carrier Boards tailored for RFSoC modules
- Support for **JESD204B/C, SFP+, QSFP**, and high-speed data interfaces
- Precision in signal integrity, impedance control, and power distribution

ADC/DAC Integration Expertise

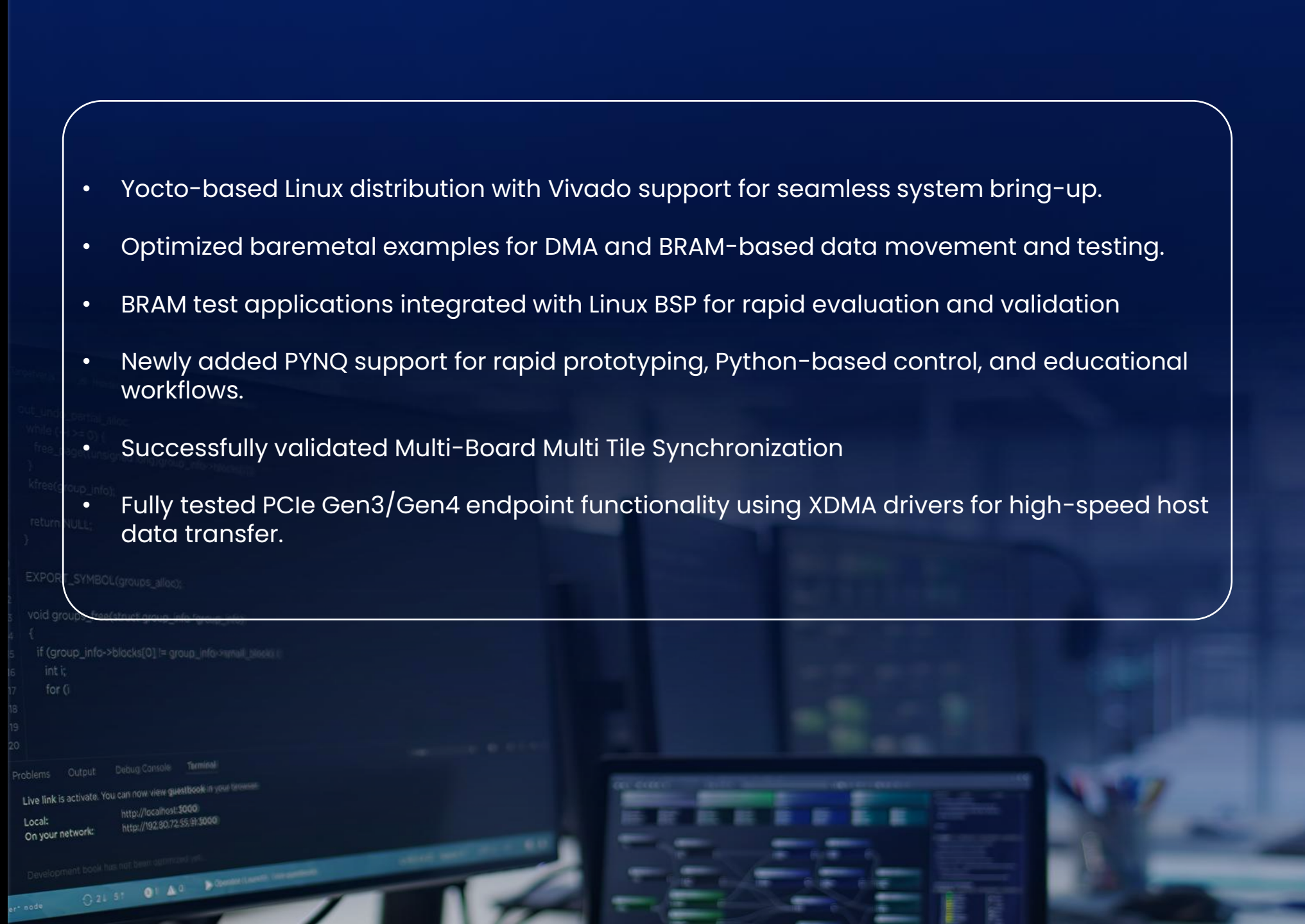
- Proven experience integrating **direct-RF ADCs/DAC** integration with Xilinx RFSoC architecture
- Optimized clock tree design with **low-jitter PLLs** and synthesizers
- Support for **wideband RF signal** capture and generation
- Implementation of **Multi-Tile Synchronization (MTS)** for phase alignment across multiple tiles
- Capability **for Multi-Board Sync** to align RF signals across multiple RFSoC devices

Production & System-Level Support

- **Turnkey Production Services** including SoM + Carrier + Enclosure + Testing
- DFM (Design for Manufacturing) and DFT (Design for Test) best practices followed
- **Ruggedization and MIL-grade validation** for Aerospace & Defense customers
- Product Longevity Support of up to **15+ Years**

Software Features

- Yocto-based Linux distribution with Vivado support for seamless system bring-up.
- Optimized baremetal examples for DMA and BRAM-based data movement and testing.
- BRAM test applications integrated with Linux BSP for rapid evaluation and validation
- Newly added PYNQ support for rapid prototyping, Python-based control, and educational workflows.
- Successfully validated Multi-Board Multi Tile Synchronization
- Fully tested PCIe Gen3/Gen4 endpoint functionality using XDMA drivers for high-speed host data transfer.



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Evaluation Platforms

Available in 3/4th length PCIe form factor

Up to 16 ADC channels with –

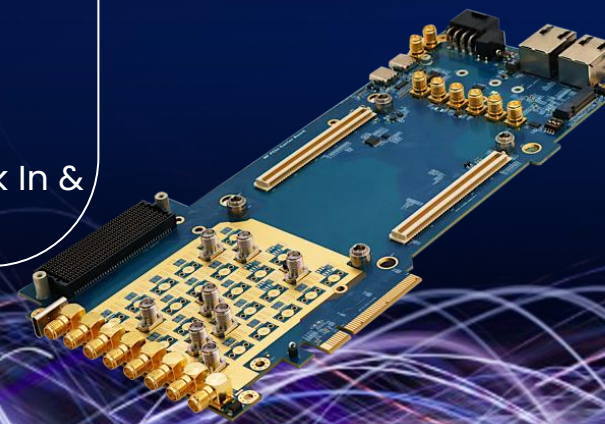
- 1 x Right Angle SMA connector on Front Panel with Balun (BW 10MHz To 3GHz)
- 3 x Right Angle SMA connectors on Front Panel with Balun (BW 3.1GHz To 5.8GHz)
- 3 x Straight SMA connectors with Balun (BW 10MHz To 3GHz)
- 9 x Straight SMA connectors with Balun (BW 3.1GHz To 5.8GHz)

Up to 16 DAC channels with –

- 1 x Right Angle SMA connector on Front Panel with Balun (BW 10MHz To 3GHz)
- 3 x Right Angle SMA connectors on Front Panel with Balun (BW 3.1GHz To 5.8GHz)
- 3 x Straight SMA connectors with Balun (BW 10MHz To 3GHz)
- 9 x Straight SMA connectors with Balun (BW 3.1GHz To 5.8GHz)

Clock & PLL –

- Integrated Configurable ultra-low noise PLL for ADC & DAC
- Fully Configurable Clock Synthesizer with SyncE and PTP support
- 4 x SMA Straight connector for clocks (10Mhz IN, 1PPS IN, Synchronous Clock In & Out)



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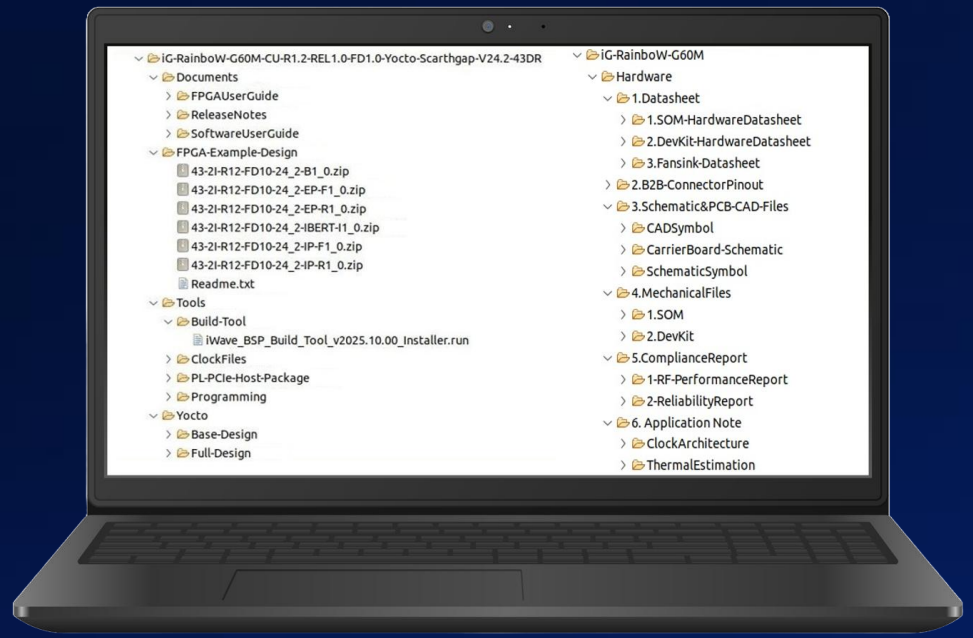
Deliverables

- **iWave BSP build tool is provided to automate the Yocto build process.**
  - GUI interface support
  - One click Initializing the host environment
  - Option to select different AMD SoC
- **FPGA designs**
  - MTS design(multi-board)
  - BRAM + PCIe based Design
  - RF Analyzer Design
  - Ibert Design
  - Base Design(PS only)
- Regular BSP updates and enhancements
- Dedicated technical support channel



SDR Framework

A ready-to-deploy software-defined radio framework built on iWave RFSoC SoMs, combining wideband RF capture, FPGA acceleration, and host-based SDR ecosystems

Wideband RF & Signal Processing

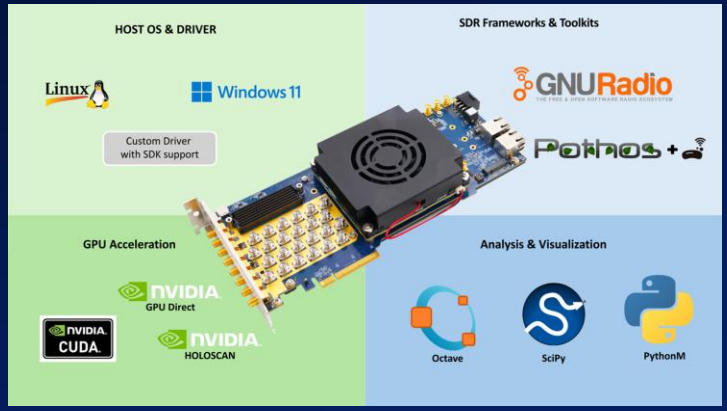
- Up to 8 independent RF channels, 14-bit resolution
- ADC: Up to 5 GSPS, DC–2.5 GHz wideband acquisition
- DAC: Up to 10 GSPS, DC–5 GHz wideband signal generation
- Multi-Tile Synchronization (MTS) with SYSREF support
- FPGA-based interpolation, decimation, and real-time DSP inside RFSoC

Software & SDR Ecosystem

- Custom host drivers with SDK support
- Dynamic control of RF frequencies, bandwidths, and multi-channel I/O
- GNU Radio–based SDR framework for rapid waveform development

Host Integration & Hardware Platform

- PCIe Gen3 x8 interface (up to 64 Gbps theoretical bandwidth)
- Full-Height Half-Length (FHHL) PCIe card form factor
- Host requirements:
  - Linux (Ubuntu 20.04+) / Windows 11
  - 8-core CPU minimum, 16 GB RAM



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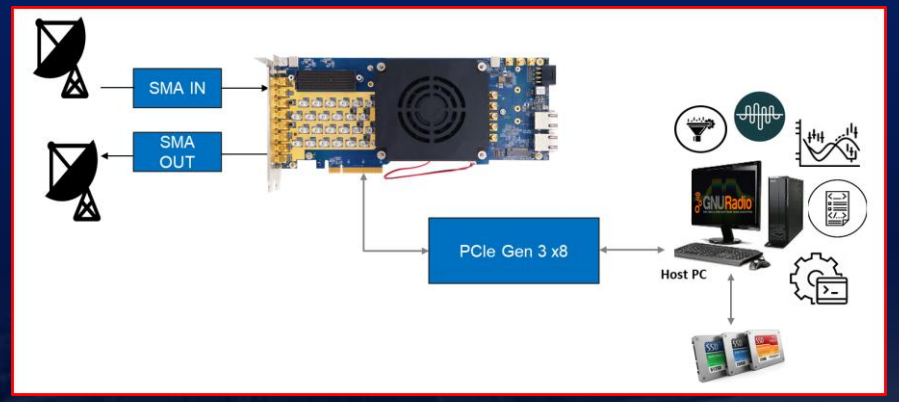
Case Study

Software Defined Radio (SDR) Framework with GNU Radio

This case study demonstrates a SDR framework built on an iWave ZU48DR RFSoC System on Module, combining direct RF sampling with programmable digital signal processing and software control.



Using the RFSoC's high-speed ADCs and DACs, wideband RF signals are directly digitized and generated without external frequency conversion stages. The integrated FPGA fabric implements real-time DSP functions such as filtering, modulation, and demodulation, while the embedded processors interface with GNU Radio for waveform control, visualization, and rapid reconfiguration.

The solution highlights a compact, low-latency SDR architecture that simplifies RF design while enabling flexibility through software. It is well suited for SDR prototyping, wireless research, defense communications, and next-generation RF systems.

Key Capabilities:

- Wideband RF sampling and generation using RFSoC ADC/DACs
- Real-time DSP acceleration in FPGA fabric
- Software-controlled SDR using GNU Radio
- Scalable architecture for multiple RF applications

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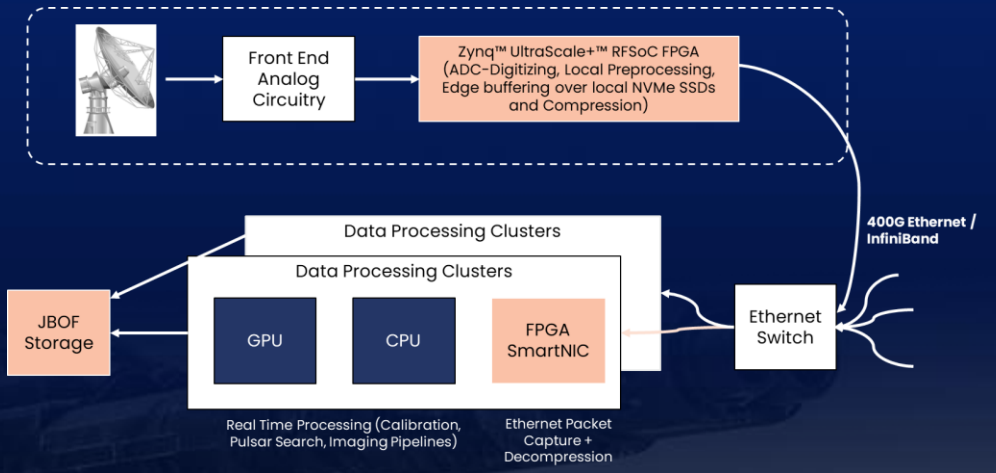
Case Study

Radio Astronomy using Zynq UltraScale+ RFSoC

This case study demonstrates a low-latency radio telescope signal processing pipeline built using an RFSoC-based RF front end integrated with an iWave SmartNIC for high-throughput data transport and acceleration.

Wideband RF signals are directly digitized using the RFSoC's high-speed ADCs and processed in the programmable logic for channelization and formatting. The processed data streams are then transferred to an iWave SmartNIC, which performs line-rate packetization, protocol offload, and deterministic transport to host compute resources with minimal CPU involvement. Downstream correlation and imaging workloads can be executed on CPUs, GPUs, or FPGA accelerators without becoming data-movement bound.



This RFSoC–SmartNIC architecture enables scalable, synchronized, and low-latency RF data pipelines, well suited for large radio astronomy arrays and next-generation telescope backends.

Key Capabilities:

- Direct RF sampling and preprocessing on RFSoC
- High-throughput RF data streaming via SmartNIC offload
- Low-latency, deterministic transport with reduced CPU load
- Scalable architecture for multi-antenna radio telescope systems

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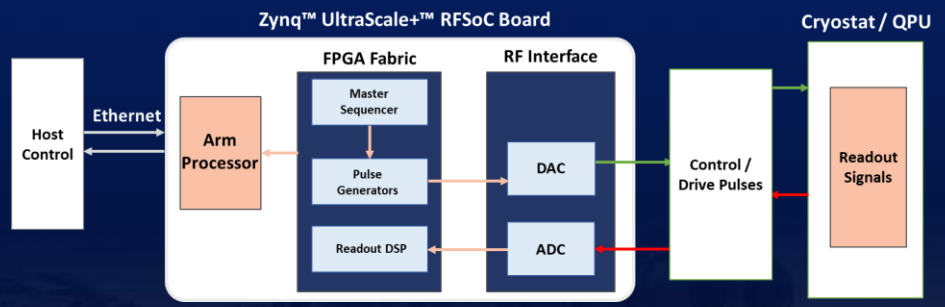
Case Study

Quantum Computing Control Unit using Zynq UltraScale+ RFSoC

This case study illustrates how an RFSoC-based control unit can be used as the real-time interface between a host quantum control system and the cryostat housing the qubits.

In this architecture, researchers develop quantum algorithms on a host system using a quantum software kit. Control data is then transferred to the RFSoC board, where software frameworks such as QICK run on the embedded processors. A master sequencer on the RFSoC generates precise timing and control sequences based on Python-defined instructions, while the pulse generator produces deterministic RF waveforms to manipulate qubit states inside the cryostat. The readout DSP pipeline processes the returned signals in real time to measure and validate qubit states.



By combining direct RF generation, low-latency processing, and tight timing control in a single platform, the RFSoC enables scalable, deterministic quantum control and readout, making it well suited for next-generation quantum research systems.

Key Capabilities:

- RFSoC positioned between host control and cryostat
- Python-driven quantum control using QICK or similar frameworks
- Deterministic pulse generation for qubit manipulation
- Real-time readout DSP for qubit state validation

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Case Study

Electronic Warfare (EW)
Radar Warning Receiver

This case study demonstrates an RFSoC-based Radar Warning Receiver (RWR) architecture for electronic warfare applications, enabling real-time threat detection and response.

In this system, wideband RF signals captured by the RF front-end analog circuitry are streamed into the RFSoC, where the on-chip high-speed ADCs digitize the incoming signals. The FPGA fabric performs channelization, pulse detection, and Pulse Descriptor Word (PDW) generation with deterministic latency. Processed data is then passed to the Arm processing subsystem, where threat libraries classify emitters and identify potential radar threats. Based on this analysis, actionable outputs are generated to drive pilot displays or countermeasure trigger systems.

By combining RF sampling, real-time FPGA processing, and embedded software on a single platform, the RFSoC enables a compact, low-latency, and highly integrated RWR solution suitable for modern EW systems.

Key Capabilities:

- Wideband RF capture and digitization using RFSoC ADCs
- Real-time channelization and pulse detection in FPGA fabric
- Threat classification using Arm-based software libraries
- Deterministic outputs for countermeasure and alert systems

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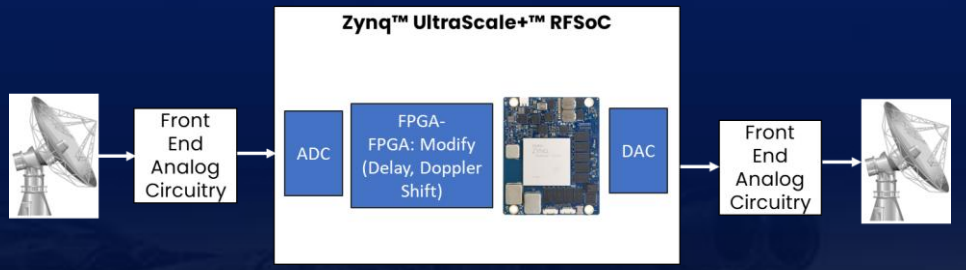
Case Study

Electronic Warfare (EW)
DRFM Jammer

This case study highlights an RFSoC-based Digital RF Memory (DRFM) Jammer designed for low-latency electronic attack applications.

Incoming wideband radar signals are captured using the RFSoC's high-speed ADCs with I/Q sampling. The digitized data is buffered in external DDR memory and processed in real time within the FPGA fabric, where delay insertion, Doppler shift, and amplitude/phase modulation are applied to generate deceptive jamming waveforms. The modified signals are then retransmitted through the on-chip DACs, enabling a tightly coupled, low-latency capture-to-transmit path. By integrating ADC, FPGA processing, memory interfaces, and DAC within a single device, the RFSoC enables sub-microsecond response times, critical for modern EW jamming scenarios.



Key Capabilities:

- Wideband I/Q signal capture using RFSoC ADCs
- DDR-based buffering for real-time signal replay
- FPGA-based delay, Doppler, and modulation processing
- Low-latency re-transmission via integrated DACs
- Deterministic, latency-critical jamming architecture

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Case Study

Electronic Warfare (EW)
SIGINT / ELINT Receiver

This case study demonstrates an RFSoC-based wideband SIGINT / ELINT receiver designed for real-time interception and analysis of unknown RF emitters.

Wideband signals are captured directly from the antenna using the RFSoC's full Nyquist ADCs covering DC to 4.4 GHz. The FPGA fabric performs digital down-conversion (DDC) and polyphase DFT-based channelization, enabling separation of multiple signals across the spectrum. Parallel demodulation chains implemented in the FPGA support AM, FM, PSK, and FSK signal types simultaneously. Higher-level signal analysis, modulation classification, and parameter extraction are handled by the integrated Arm processing system. Captured data can be stored locally using high-speed NVMe storage or streamed in real time over ultra-high-speed interfaces such as 400G Ethernet to external processing systems.

Key Capabilities:

- Full Nyquist wideband capture from DC to 4.4 GHz
- Polyphase DFT filter bank for multi-channel frequency separation
- Parallel FPGA-based demodulation of multiple modulation schemes
- Arm-based signal classification and feature extraction
- High-speed storage and network streaming for downstream analytics

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Resources

Technical Articles

- Article – RFSoC for Electronic Warfare (EW): Wideband Sensing and Real-Time Jamming Solutions
- Article - oHFM Standard Explained: Enabling Scalable FPGA System on Modules
- Press Release –Introducing Versal™ RF Series SoM featuring Integrated AIE
- Article – Enabling Sub-Nanosecond Synchronization in Distributed MPSoC & RFSoC SOM using White Rabbit Protocol
- Article - A Unified Software and Acceleration Stack for High-Performance SDR Systems
- Article - Why FPGA-Based Platforms Power Next-Generation Software Defined Radio (SDR)
- Article - Real-Time Quantum Control Using QICK on iWave Zynq™ UltraScale+™ RFSoC SOM
- Article - A Unified Software and Acceleration Stack for High-Performance SDR Systems
- Article - How to choose the right RFSoC Variant for your RF and Wireless application
- Press Release - ZU67/65/64/63DR Zynq™ UltraScale+™ RFSoC DFE RFSoC SOM Product Launch
- Article – Why Multi Tile Synchronization (MTS) is essential for Radio Telescope Systems
- Article - Designing Software Defined Radio (SDR) with RFSoC SoM
- Article – Achieving Deterministic Phase alignment in Multi-Tile RFSoC Systems
- Article – Implementation of PYNQ on AMD Zynq UltraScale+ RFSoC
- Article – RFSoC System on Module for Satellite Communication and Aerospace

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Resources

Case Studies

- Case Study – Electronic Warfare System Using Zynq UltraScale+ RFSoC SOM
- Case Study - Quantum Control Unit Using Zynq UltraScale+ RFSoC System on Module
- Case Study – Software Defined Radio using ZU48DR RFSoC based Solution
- Case Study – Photonic Computing using ZU49DR RFSoC PCIe Card
- Case Study - Radio Telescope using ZU49/ZU39/ZU29DR Zynq UltraScale+ RFSoC SoM
- Case Study – Electronic Warfare using Zynq UltraScale+ RFSoC System on Modules

White Paper

- White Paper – Accelerating Next-Gen SDR Systems with Zynq™ UltraScale+™ RFSoC

Videos

- WEBINAR: RF System Design with AMD Zynq UltraScale+ RFSoC, Versal RF Series & iWave RF Solutions
- Overview Video: Explore iWave's Zynq UltraScale+ RFSoC SoMs & 3U VPX Cards
- Overview Video: RFSoC System on Module from iWave and its Key Features
- Demo: DAC to ADC Loopback using RF Analyzer on ZU49DR RFSoC Evaluation Kit from iwave | Part 2
- Unboxing ZU49DR RFSoC SoM Evaluation Kit from iWave | Part 1
- Demo: Achieving Multi-Board MTS Synchronization with ZU49DR RFSoC SoM

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Thank You

We are here to
Accelerate Embedded Innovation

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